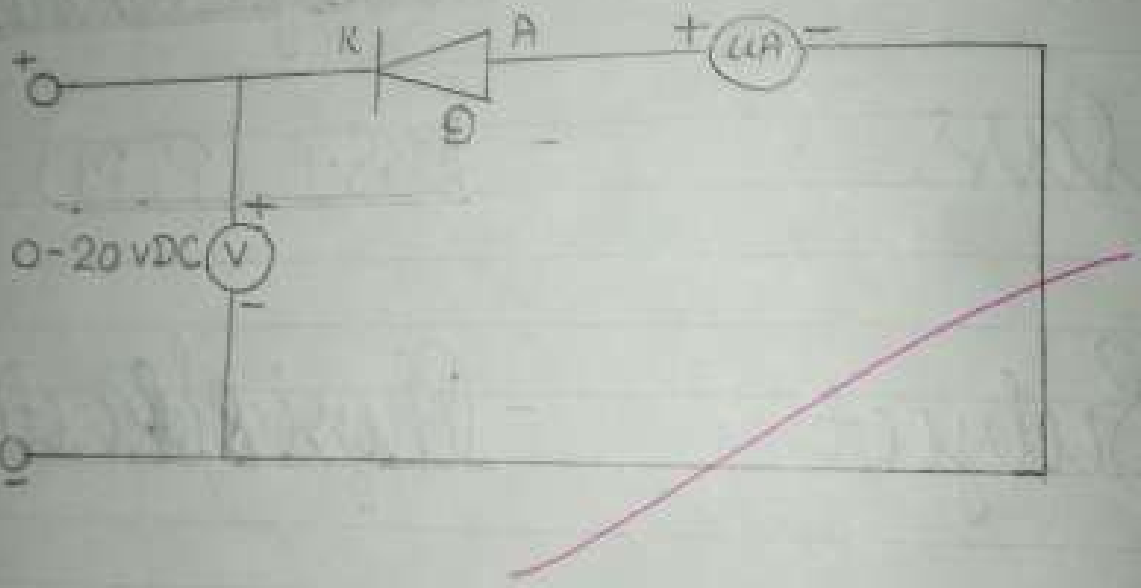
K
A
G
+
uA
−
+
0-20 vDC
V
−
+
−

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Experiment - 1

Objective - Energy band gap of Semiconductor by Reverse saturation current method.

Apparatus used - One Variable (DC) Regulated Power Supply. Two meters to measure voltage, reverse saturation current. Temperature controlled electric oven, mercury thermometer electric oven, PN Junction diode, connection wire.

Theory - We know in the case of insulators, the region between highest completely filled band (called conduction band) is very wide. This is energy gap. This is denoted by Eg and is about 3 to 7 ev (electron volt) in case of insulators.

In case of Semiconductors, this energy gap is quite small for examples in case of Germanium Eg = 0.7ev and in case of silicon Eg = 1.17ev

In semi-conductors at low temperatures, there are few charges to move so conductivity is quite low. At higher temperatures the donor or acceptor levels come into action and provide carriers and hence the conductor rises. In addition to

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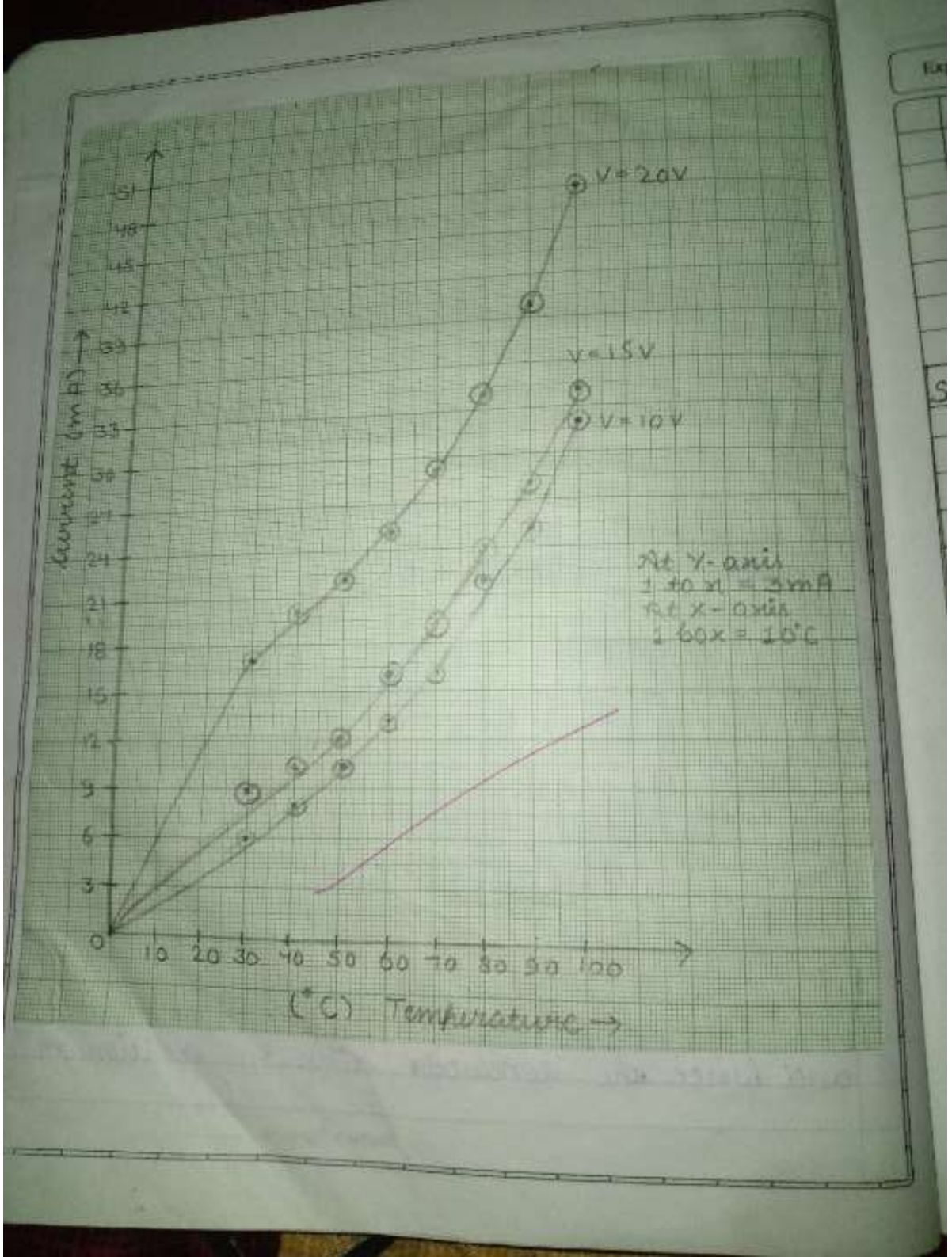
V = 20V
V = 15V
V = 10V
Current (mA)
51
48
45
42
39
36
33
30
27
24
21
18
15
12
9
6
3
0
10 20 30 40 50 60 70 80 90 100
(°C) Temperature →
At Y-axis
1 to x = 3mA
At X-axis
1 box = 10°C

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the dependence of the electrical conductivity on the number of free charges, it also depends on their mobility. However mobility of the charges carriers some what decrease with the increasing temperature.

Observation Table -

S.No	Temperature	Current (mA)		
		V=10V	V=15V	V=20V
1.	30°C	6	9	17
2.	40°C	8	10	20
3.	50°C	10	12	22
4.	60°C	13	17	25
5.	70°C	16	19	29
6.	80°C	22	24	34
7.	90°C	25	28	40
8.	100°C	32	34	48

Result - Graph between Reverse saturation current and temperature for energy band gap

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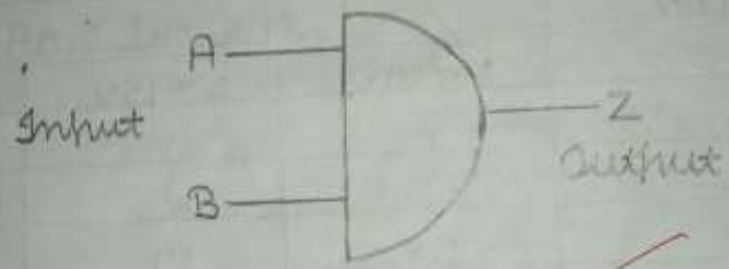

AND gate

Date 16/02/26

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Expt. No.

Experiment - 2

Object - Study and verification of AND gate using TTL IC-7408

Apparatus used - Bread board, connecting leads, LED's, IC 7408.

Theory - The AND gate performs logical multiplication. AND gate circuit has two inputs and one output. Whenever both the inputs are high or 1 the output for this will be logic high or 1 and low otherwise. The truth table for AND gate is;

Inputs		Output
A	B	Z
0	0	0
0	1	0
1	0	0
1	1	1

Result - The Operation of logic gate is successfully verified.

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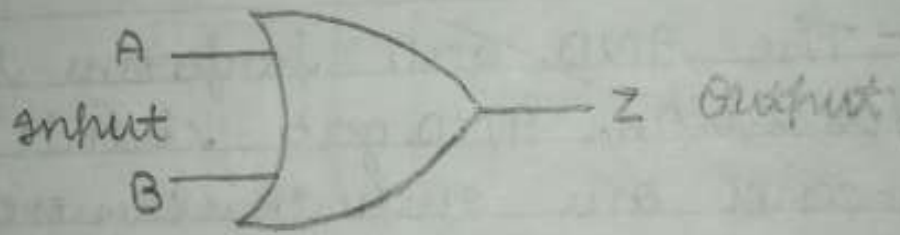

OR gate

Date 10/02/26

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Experiment - 3

Object - Study and verification of OR gate using TTL IC 7432

Apparatus used - Bread board, connecting leads, LED's, IC 7432.

Theory - The OR gate performs logical addition OR gate circuit has two inputs and one output whenever both the inputs are low or 0 the output for this will be logic low or 0 and high or 1 otherwise. The truth table for OR gate is

Inputs		Output
A	B	Z
0	0	0
0	1	1
1	0	1
1	1	1

Result - The operation of logic gate is successfully verified.

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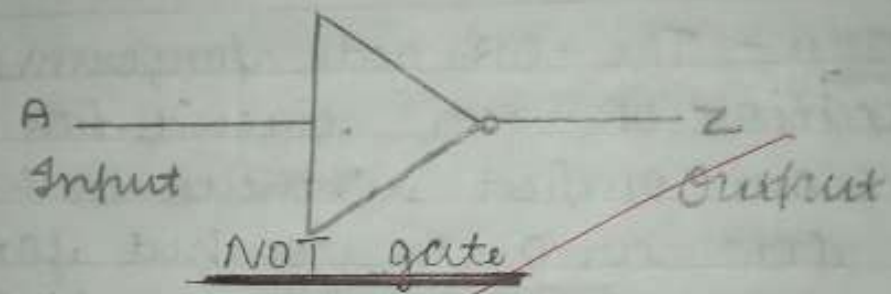
A
Input
Z
Output
NOT gate

Experiment - 4

Object - Study and verification of NOT gate using TTL IC 7404.

Apparatus used - Bread board, connecting leads, LED's, IC 7404.

Theory - The inverter (NOT circuit) perform a basic logic function called inversion or complementation. This gate has only one input and one output. NOT gate is called the inverter, because output state is always opposite to the input state. When the input is low or 0, the output is logic high or 1 and voice versa.

Input	Output
0	1
1	0

Result - The operation of logic gate is successfully verified.

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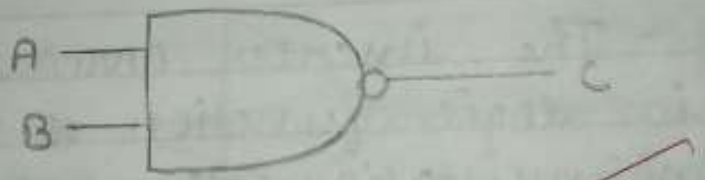

NAND gate

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Experiment - 5

Object - Study and verification of NAND gate and use as universal gate using TTL IC 7400.

Apparatus used - Bread board, connecting leads, LED's, IC 7400.

Theory - The term NAND is a contraction of NOT-AND and implies an AND function with complemented output. NAND gate has two inputs and one output. Whenever at least one of the inputs is low, the output voltage will be high. If both inputs are high, then the output logic is low. The truth table for NAND gate is

Input		Output
A	B	C
0	0	1
0	1	1
1	0	1
1	1	0

Result - The operation of logic gate is successfully verified.

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NOR gate

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Experiment - 6

Object - Study and verification of NOR gate and use as universal gate using TTL IC 7402.

Apparatus used - Bread board, connecting leads, LED's IC 7402.

Theory - The term NOR is a contraction of NOT-OR and implies an OR function with an inverted output. The circuit has two inputs and one output. whenever at least one of the input is high or 1, the output will be low or 0. If both inputs are low, then output is high or 1. The truth table for NOR gate is

Input		Output
A	B	C
0	0	1
0	1	0
1	0	0
1	1	0

Result - The operation of logic gate is successfully verified.

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Ex-OR gate

Date 16/02/26

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Experiment - 7

Object - Study and verification of Ex-OR gate using TTL IC 7486.

Apparatus used - Bread board, connecting leads, LED's IC 7486.

Theory - Ex-OR gate circuit has two inputs and one output. Whenever both the inputs are the same, the corresponding output will be low otherwise the output will be logic high or 1. The truth table for Ex-OR gate is;

Input		Output
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

Result - The operation of logic gat is successfully verified.

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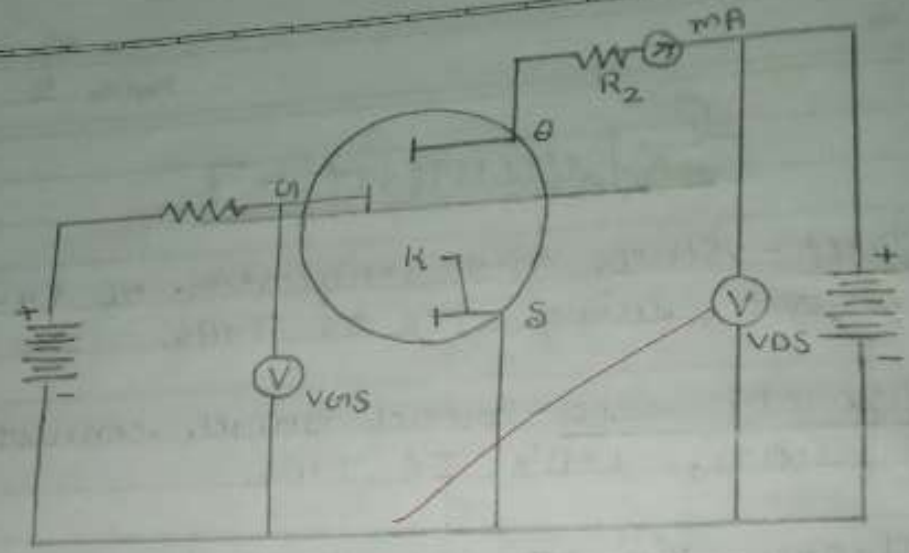
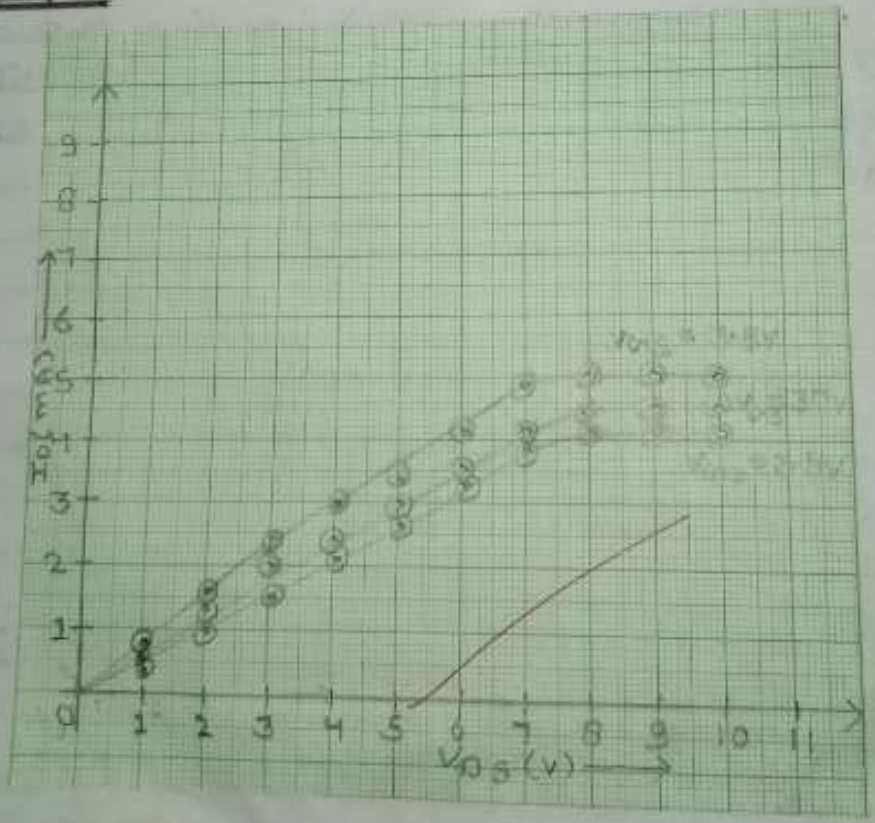


Graph-



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Experiment - 8

Object - To study the characteristics of MOSFET.

Apparatus used - MOSFET, resistors, connecting wires, ammeter, voltmeter, dc power supply etc.

Theory - A MOSFET (Metal-oxide Semiconductor field-effect transistor) is a voltage-controlled three terminal device (source, drain and gate) that use an electric field generated by the gate voltage to modulate the conductivity between the source and drain, controlling current flow. N-channel MOSFET, P-channel MOSFET, Enhancement mode, Depletion mode.

Observation - a) Output (drain) characteristics

V_{GS} (Volts)	V_{DS} = 3.5V	V_{DS} = 3.7V	V_{DS} = 3.8V
	I_D (mA)	I_D (mA)	I_D (mA)
0	0	0	0
1	0.5	0.6	0.4
2	1.3	1.5	0.9
3	1.9	2.3	1.6
4	2.4	2.9	2.4

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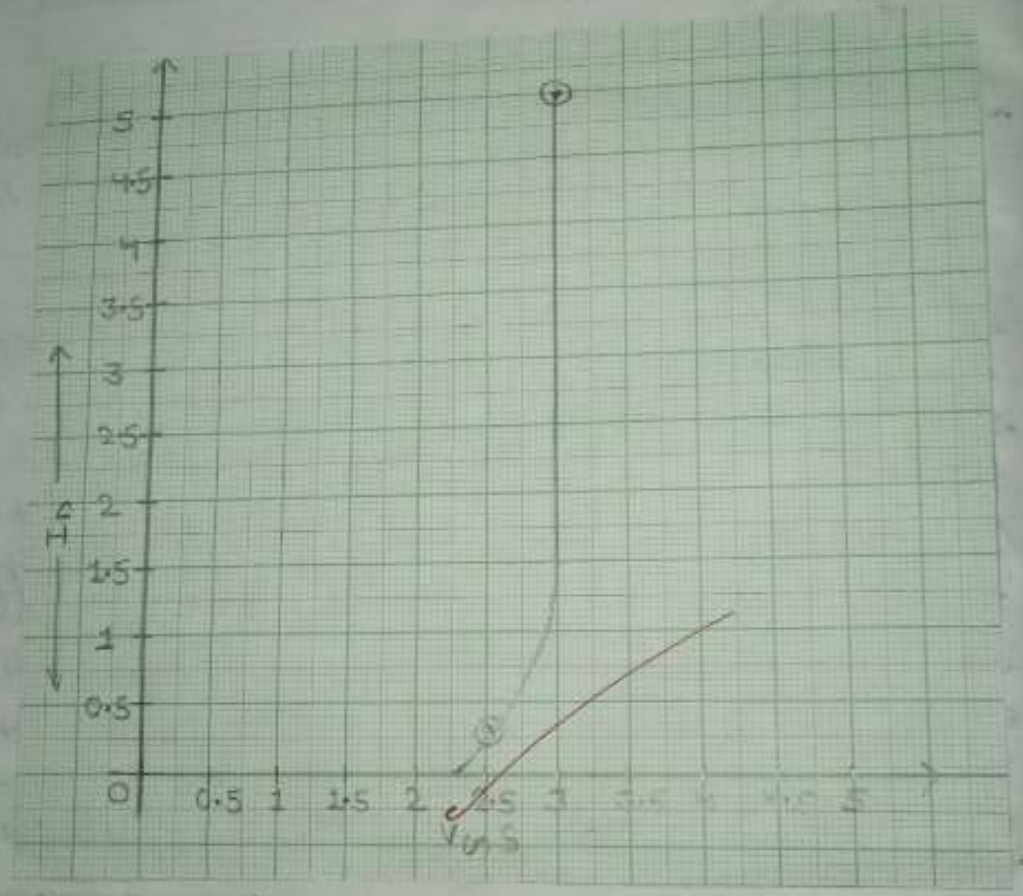
Graph -



5	3	3.3	2.9
6	3.5	4.1	3.5
7	4.2	4.7	4.3
8	4.5	5	4.7
9	5	5	5
10	5	5	5

(b) Transfer characteristics

	V_{DS} = 20V	
	V_{GS}	I_{DS}
1	0	0
2	0.5	0
3	1	0
4	1.5	0
5	2	0
6	2.5	0.3
7	3	5

Result - The characteristics of MOSFET has been plotted.

Precaution - (1.) All the wire connections should be proper.

2) The device should be handled carefully.

3) There should never be connected or disconnect when the power is ON.

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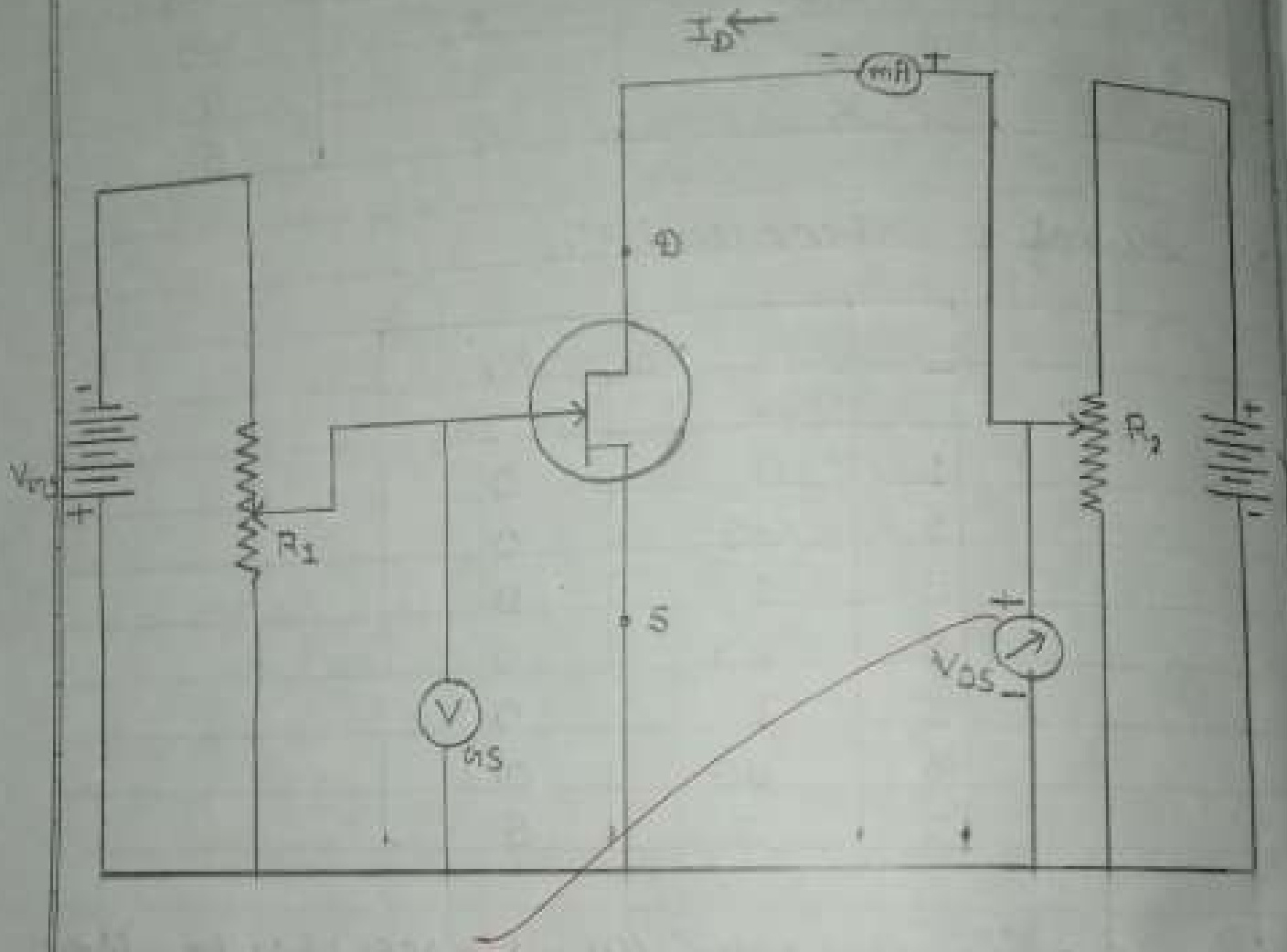
I_D
mA
D
S
R_1
R_2
V_{GS}
V
V_{DS}

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Experiment - 9

Object - To plot the V-I characteristics of F.E.T different gate voltage.

Apparatus used - F.E.T experimental connection wires.

Theory - The field effect Transistor or Junction field effect Transistor is fabricated by using monolithic Silicon technology. This device comprises of high input resistance as compared to bipolar transistor. FET's are mainly of two types.

1. Junction field effect Transistor (JFET).
2. Metal - Oxide Semiconductor field effect Transistor (MOSFET).

Observation Table → (A)

SR No.	V_{DS} (volts)	I_D (mA) For $V_{GS} = 0V$	$V_{GS} = 0.25V$	$V_{GS} = 0.5V$
0	0	0	0	0
1	2.5	2.5	1.75	0
2	5	5	2.75	0.25
3	7.5	6.75	3.25	0.50

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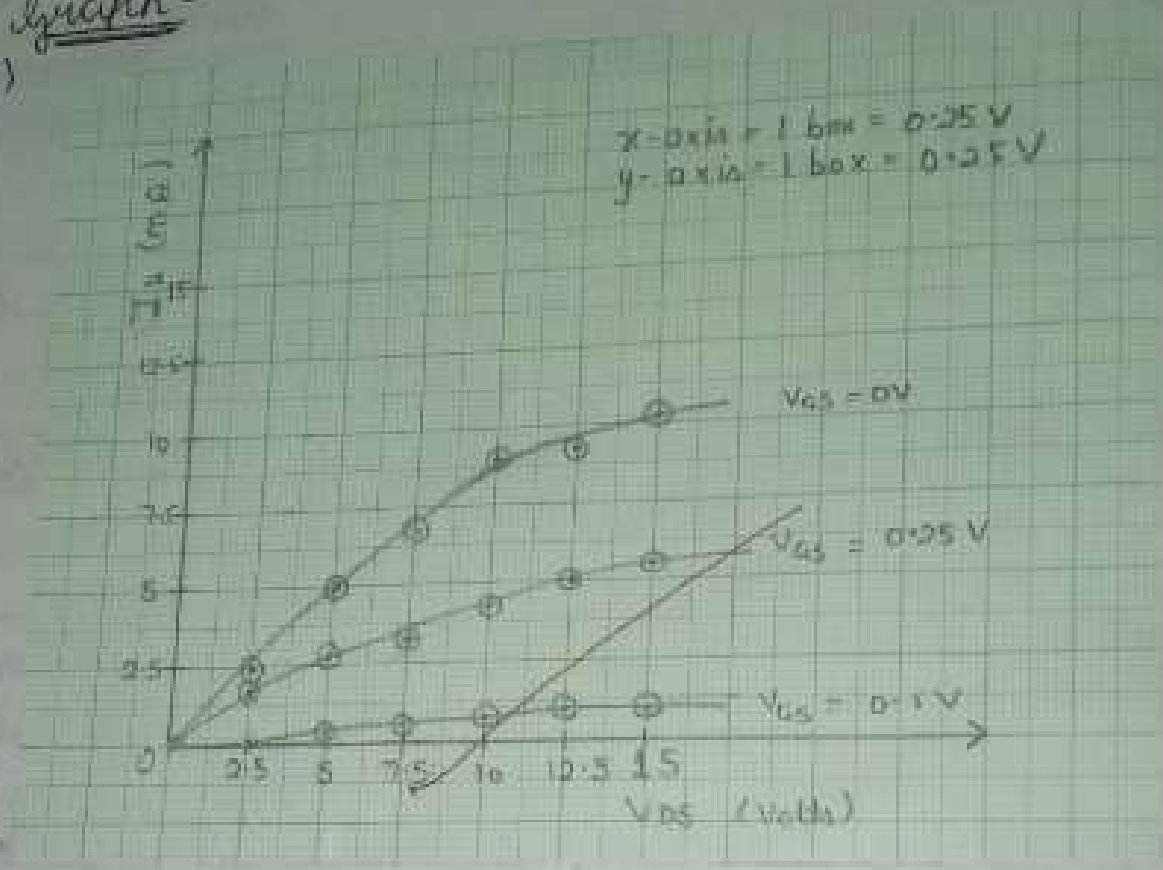
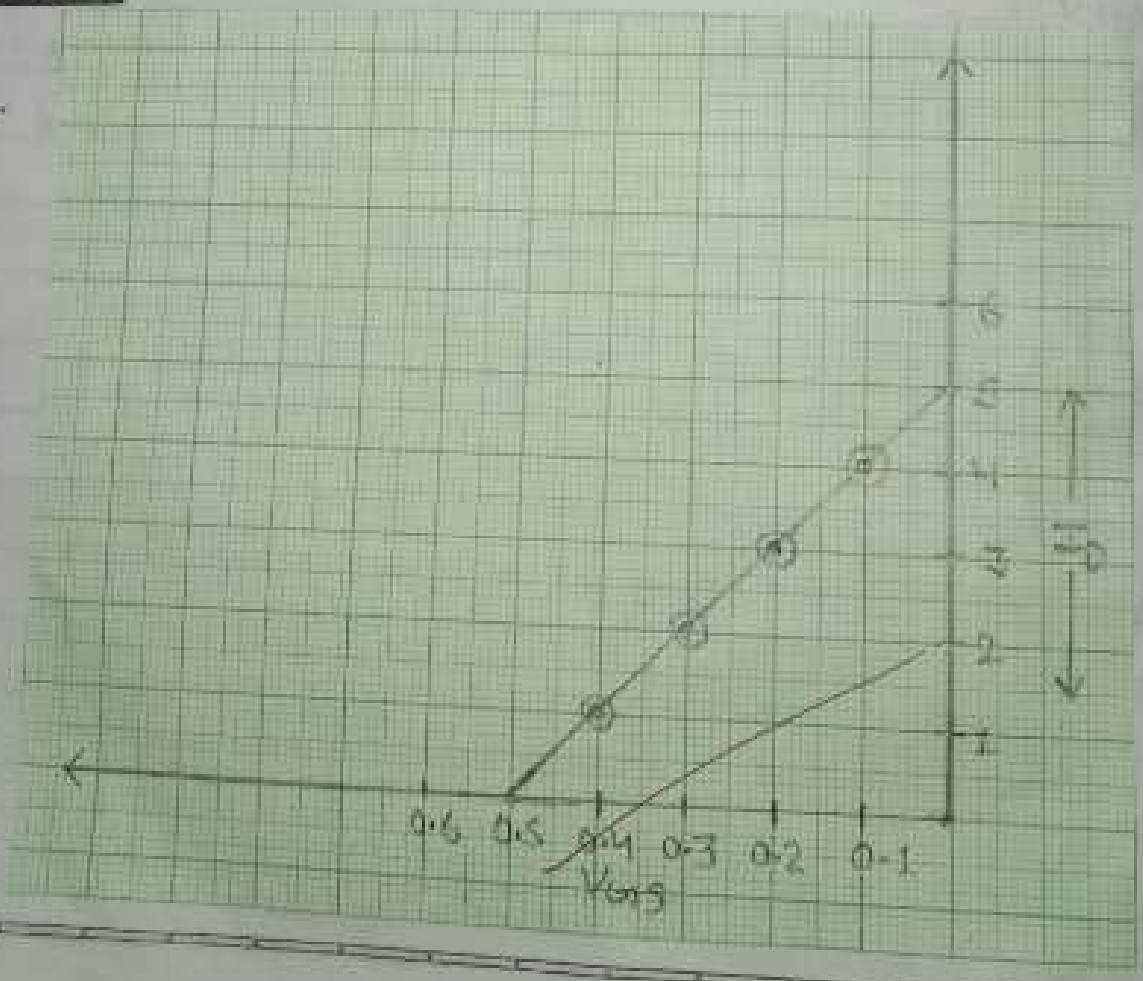
(A) Graph -



(B) Graph -



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4	10	8.25	4.25	0.75
5	12.5	9.25	5	1.00
6	15	10.25	5.50	1.00

(B)

S.R NO.	For constant V_{DS} = 5V.	
	V_{GS} (Volts)	I_D (mA)
1	0	5
2	0.1	4.25
3	0.2	3.25
4	0.3	2.00
5	0.4	1.00
6	0.5	0

Result - The characteristics of F.E.T have been plotted graph.

Precaution - (1) All the wire connections should be proper.

(2) The device should be handled carefully.

(3) These should never be connected or disconnect when the power is ON.

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Experiment - 10

Object - Study of characteristics of UJT.

Apparatus Required - Power supply, UJT characteristics, connecting leads, Ammeter, Voltmeter.

- **Theory** - A Uni junction transistor is a three terminal semiconductor device having two doped regions. In the three terminals, it has one emitter (E) & two Bases (B_1 & B_2). It has only one junction. It consist of an n-type silicon bar which is lightly doped. Two end connections are taken from the bar called B_1 & B_2. A heavily doped P-region is diffused to n-bar nearer to B_2.

- **Observation Table** -

$$V_{B_2B_1} = 10\ V$$

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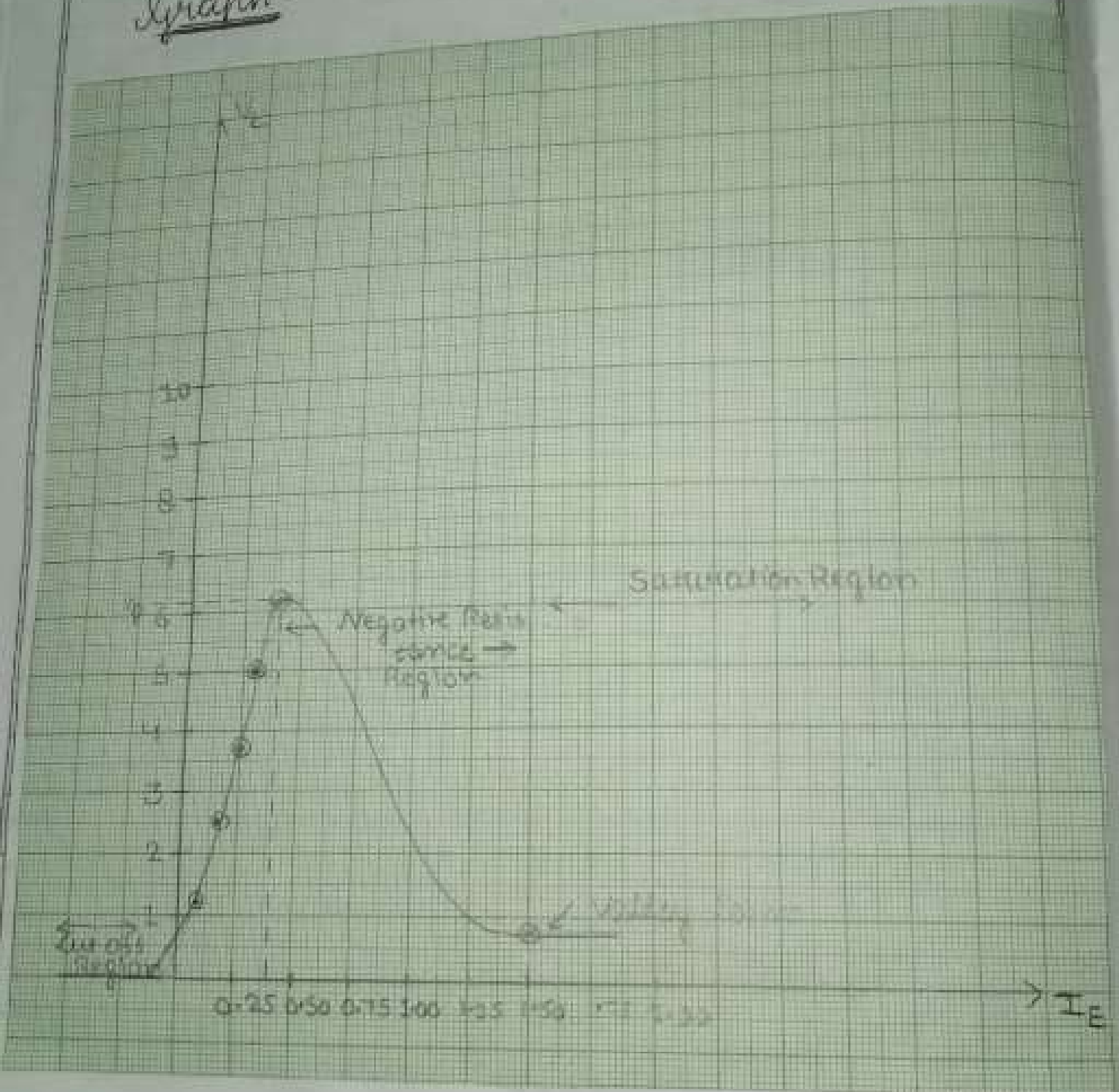
Graph-


Saturation Region
Negative Resistance Region
Valley point
I_E

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UJT characteristics

S.NO	V (volts)	I (mA)
1	1.25	0.075
2	2.5	0.15
3	3.75	0.25
4	5	0.325
5	6.25	0.4
6	0.75	1.5

- **Result** - The characteristics of UJT have been plotted.

- **Precaution** -

(1) Always connect the voltmeter in parallel & ammeter in series as shown in fig.
(2) Connection should be proper & tight.
(3) Switch 'ON' the supply after completing the ckt.
(4) DC supply should be increased slowly in steps.
(5) Reading of voltmeter & ammeter should be accurate.

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